REMARKS

Claims 40-58 are pending in the application with claims 40-42, 48-50, 56, and 58 amended herein.

Claims 40-58 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 6,611,059. Applicant submits herewith a timely filed terminal disclaimer obviating the need for such rejection. Applicant thus requests withdrawal of the obviousness-type double patenting rejection.

Claims 40-58 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Applicant herein amends claims 40-42 to make usage of the terms "first and second conductive lines" consistent within such claims. Applicant herein amends claims 48-50 to make usage of the terms "first and second conductive lines" consistent within such claims. Applicant herein amends claims 56 and 58 to make usage of the terms "first and second series conductive lines" and "insulative oxide material" consistent within such claims. Applicant requests withdrawal of the indefiniteness rejection in the next Office Action.

Claims 40-55 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lur in view of Choe. Applicant requests reconsideration.

Amended claim 40 sets forth integrated circuitry including, among other features, a series of alternating first and second conductive lines spaced and positioned laterally adjacent one another over an electrically insulating layer over a semiconductive substrate. The series of first conductive lines or the series of second conductive lines provide cross-talk shielding for the other series. Page 4 of the Office Action alleges that Lur teaches every limitation of claim 40 except for intervening insulating spacers

electrically isolating the first conductive lines and the second conductive lines. Applicant traverses.

Page of the Office Action states that polysilicon conductors 24 discussed in column 4 and shown in Fig. 11 of Lur disclose the claimed series of alternating first and second conductive lines. Claim 40 states that the series of alternating first and second conductive lines are spaced and positioned laterally adjacent one another. As known to those of ordinary skill, "adjacent" means close to, lying near, next to, or adjoining. One advantage of the integrated circuitry set forth in claim 40 is that the lateral adjacency of the two series and their electrical isolation allows the series of first conductive lines or the series of second conductive lines to provide cross-talk shielding for the other series, as set forth on page 7, line 24 to page 8, line 9 of the present specification. As may be understood from the referenced portion and elsewhere throughout the present specification, the structural relationships between the first and second conductive lines set forth in claim 40 enable the desired advantages. As may be understood of those of ordinary skill, first and second conductive lines that are not spaced and positioned laterally adjacent one another might not provide cross-talk shielding, as claimed.

Review of Lur reveals that polysilicon conductors 24 are separated from one another by sidewall spacers, base dielectric layer 30, and contact studs 26. The spacing and positioning shown in Fig. 11 can hardly be considered to disclose polysilicon conductors 24 as "laterally adjacent." Further, it is apparent that polysilicon conductors 24 are not provided sufficiently laterally adjacent to provide cross-talk shielding. Lur does not disclose or suggest any such property. At least for such reasons, Lur fails to disclose every limitation of claim 40.

In addition, claim 40 sets forth a "series" of alternating first and second conductive lines. Lur does not show in Fig. 11 or discuss elsewhere throughout the text of such reference any "series" of alternating first and second conductive lines. Lur only describes two lines which do not disclose a "series of alternating" first and second conductive lines. Even if the two polysilicon conductors 24 or some other conductors found to be disclosed by Lur could be considered a series of alternating first and second conductive lines, such alleged lines are not disclosed or suggested as possessing the other structural features set forth in claim 40. At least for such additional reason, Lur fails to disclose every limitation of claim 50.

Further, page 4 of the Office Action relies upon Cho as allegedly disclosing insulating spacers. However, Cho does not disclose or suggest and is not alleged to disclose or suggest the subject matter of claim 40 that is absent from Lur. Combination of references cannot be considered to disclose or suggest subject matter that is absent from both. At least for such reason, claim 40 is patentable over Lur in view of Cho.

Claims 41-47 depend from claim 40 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, claim 44 sets forth that the first and second conductive lines constitute different materials. Page 5 of the Office Action alleges that polysilicon conductors 24 disclose the first conductive lines and first electrode metal layer 40 discloses the second conductive lines. However, polysilicon conductors 24 and first electrode metal layer 40 are not spaced and positioned laterally adjacent one another, as set forth in claim 40 from which claim 44 depends. Accordingly, Lur does not disclose or suggest the subject matter of claim 44. Claims 45 and 46 set forth that the first conductive lines contain polysilicon and the second conductive lines contain metal. However, as may be

appreciated from the deficiencies of Lur as applied to claim 44, Lur fails to disclose or suggest the subject matter of claims 45 and 46.

Amended claim 48 sets forth integrated circuitry that includes, among other features, a series of alternating first and second conductive lines over a layer of electrically insulating material over a semiconductive substrate. The first and second conductive lines have respective lateral widths and are spaced and positioned laterally adjacent one another. The first and second conductive lines are electrically isolated and separated from one another laterally by intervening strips of insulating material only having respective individual insulating material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines. Page 6 of the Office Action alleges that Lur discloses every limitation of claim 48. Applicant traverses.

As in claim 40, the first and second conductive lines of claim 48 are also spaced and positioned laterally adjacent one another. In claim 48, the first and second conductive lines are separated by intervening strips of insulating material only having respective lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines. Review of Lur reveals that such reference does not disclose or suggest polysilicon conductors 24 as laterally adjacent one another. In addition, Lur does not disclose or suggest that the sidewall spacers on the sidewalls of polysilicon conductors 24 and base dielectric layer 30 between polysilicon conductors 24 only have lateral widths that are substantially less than the lateral widths of polysilicon conductors 24. At least for such reason, Lur fails to disclose or suggest every limitation of claim 48.

Further, as may be appreciated from the above discussion regarding the deficiencies of Lur as applied to claim 40, Lur fails to disclose or suggest a series of

alternating first and second conductive lines. The mere two polysilicon conductors 24 described in Lur do not constitute the two series set forth in claim 48. Even if some logical extension of Fig. 11 might include additional polysilicon conductors 24, no support exists within Lur for the proposition that such logical extension necessarily discloses or suggests a series of alternating first and second conductive lines. Certainly, such logical extension would fail to disclose or suggest the two series having the structural relationships set forth in claim 48. At least for such additional reason, Lur fails to disclose or suggest every limitation of claim 48.

Choe does not disclose or suggest and is not alleged to disclose or suggest the subject matter absent from Lur. Combination of references cannot be considered to disclose or suggest subject matter that is absent from both. At least for such reason, claim 48 is patentable over Lur in view of Choe. Claims 49-55 depend from claim 48 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, the cited combination of references fails to disclose or suggest the subject matter of 52-53 as may be appreciated from the above discussion regarding claims 44-46.

In keeping with Applicants assertions herein, claim 40-55 are patentable over Lur in view of Choe and Applicant requests allowance of such claims in the next Office Action.

Claims 56-58 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chu in view of Miyanaga. Applicant requests reconsideration.

Amended claim 56 sets forth integrated circuitry that includes, among other features, a series of first conductive polysilicon lines over a BPSG layer over a semiconductive substrate with the individual first series conductive lines effectively

insulated by the BPSG layer, respective sidewall spacer pairs, and respective insulative oxide material over respective first series conductive lines. A top of the insulative oxide material defines a first plane. A series of second conductive aluminum-containing lines over the BPSG layer have respective line tops at least some of which define a second plane that is coplanar with the first plane. Pages 6-7 of the Office Action allege that Chu discloses every limitation of claim 56 except for the BPSG layer and relies upon Miyanaga as allegedly disclosing the missing subject matter. Applicant traverses.

Pages 6-7 of the Office Action allege that polysilicon control gate 302, such as shown in Fig. 3H, discloses the first series conductive lines and that refractory metal layer 303 formed on and in contact with polysilicon control gate 32 discloses the second series conductive lines. As known to those of ordinary skill, aluminum clearly does not constitute a refractory metal. Accordingly, Chu fails to disclose or suggest a series of second aluminum-containing lines. Commonly, refractory metals include Mo, W, Ta, Ti, Re, and Nb.

Also, page 6 of the Office Action states that insulating layer 304 over refractory metal layer 303 discloses the electrically insulative oxide material set forth in claim 56. In such case, it is impossible for the first plane and second plane of Chu to be coplanar. Insulating layer 304 has a top that defines a first plane that is elevationally higher than a top of refractory metal layer 303 defining a second plane. Since the two planes are at different elevational levels, it is impossible for them to be coplanar. Accordingly, Chu fails to disclose or suggest every limitation of claim 56.

Miyanaga does not disclose or suggest and is not alleged to disclose or suggest the subject matter absent from Chu. Combination of references cannot be considered to disclose or suggest subject matter that is absent from both. Accordingly, claim 56 is

patentable over Chu in view Miyanaga. Claims 57 and 58 depend from claim 56 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

As asserted herein, claims 56-58 are patentable over Chu in view of Miyanaga and Applicant requests allowance of such claims in the next Office Action.

Applicant herein establishes adequate reasons supporting patentability of claims 40-58 and requests allowance of all such pending claims in the next Office Action.

Applicant expresses appreciation for receiving an initialed copy of a previously submitted IDS with the June 2, 2004 Office Action. However, Applicant notes that the article listed under AR in "Other References" was not initialed. Therefore, Applicant herewith submits a copy of the Information Disclosure Statement and Form PTO-1449 submitted on August 26, 2003 requesting examination and initialing of the referenced article and returning of a copy to the undersigned.

Respectfully submitted,

Dated: 30 Sep 2004

By: _____
James E. Lake
Reg. No. 44,854

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)

ATTY. DOCKET NO. MI22-2374	SERIAL NO. Filed Herewith
APPLICANT H. Montgomery Manning	
FILING DATE Filed Herewith	GROUP 2826

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,552,628	09/1996	Watanabe			
	AB	5,585,664	12/1996	Ito			
	AC	5,583,357	12/1996	Choe			
	AD	4,418,239	11/1983	Larson			
	AE	4,693,530	09/1987	Stillie			
	AF	4,781,620	11/1988	Tengler			
	AG	4,933,743	06/1990	Thomas			
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	AK	5,176,538	01/1993	Hansell, III			
	AL	4,686,759	08/1987	Pals			

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		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AM	JP 0097300	04/1994	Japan				
	AN	JP 054925	02/1990	Japan				
	AO							
	AP							
	AQ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		Thomas, Michael E., "VLSI Multilevel Micro-Coaxial Interconnects for High Speed Devices", 1990, IEEE, pps. 55-58.
	AS		
	AT		

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.